What is claimed is:

1. An analog to digital converter, comprising:

a plurality n of successive approximation type A/D converters, where there are at least three of said successive approximation A/D converters, arranged to receive image information in an analog form, and each of said n successive approximation type A/D converters outputting digital information at different times which are offset from one another.

2. A converter as in claim 1, wherein each A/D converter requires a plurality of clock cycles to make a single A/D conversion.

3. A converter as in claim 1, wherein each A/D converter requires n clock cycles, and wherein there are n of said A/D converters, and said offset between A/D converters is one clock cycle.

4. A converter as in claim 3 wherein n equals 12.

5. A converter as in claim 3, wherein said plurality of successive approximation A/D converters are each formed

from a plurality of unit capacitors forming a total capacitance to be used by said converter.

6. A converter as in claim 5, wherein each of said A/D converters includes a comparator, and further comprising an amplifier element located between said capacitors and said comparator.

7. A converter as in claim 1, wherein each of said successive approximation A/D converters includes a plurality of capacitors, arranged to provide values indicative of different numbers of bits, a comparator, and a buffering element coupled between said capacitors and said comparator.

8. A converter as in claim 1,wherein each of said successive approximation A/D converters includes a plurality of capacitors, arranged to provide values indicative of different bits, and a comparator which compares outputs from said capacitors with a signal value.

9. A converter as in claim 7, further comprising a calibration element, coupled to an output of said buffer and an input of said comparator.

10. A converter as in claim 5, further comprising a logic element which selects a number of said unit capacitors based on a current bit being processed.

11. A converter as in claim 10, wherein said logic element receives a system clock, and is toggled between each state and the next state by said system clock.

12. A converter as in claim 1, further comprising a logic signal producing element, which produces logic signals to cause said n successive approximation A/D converters to output said digital information at said different times.

13. A converter as in claim 12, wherein said logic signal producing elements includes a plurality of flip-flops which are driven by a system clock.

14. A method, comprising:

receiving pixel analog data from a plurality of image sensor elements; and

converting said pixel analog data to digital in a way that takes multiple clock cycles, and in a way that

staggers the output timing such that pixel data is available at each of a plurality of clock cycles.

15. A method as in claim 14, wherein said converting is such that pixel data is available at each and every clock cycle.

16. A method as in claim 15, wherein said converting takes N clock cycles to complete, and wherein there are N separate analog to digital converters, each operating staggered by one clock cycle.

17. A method as in claim 16, wherein said converting uses a comparator, and further comprising compensating for comparator kickback.

18. A method as in claim 17, wherein said compensating for comparator kickback comprises buffering between capacitors of an A/D converter, and comparators of an A/D converter.

19. A method as in claim 17, further comprising calibrating each of a plurality of individual A/D converters.

20. A method as in claim 17, wherein said converting comprises converting using successive approximation, according to values produced on a plurality of capacitors.

21. A method as in claim 20, wherein said converting comprises providing a plurality of unit capacitors, and switching different numbers of said unit capacitors depending on a stage of the bit.

22. A method, comprising:

receiving image data in a plurality of image sensor elements, which output analog data;

providing said analog data to a plurality of successive approximation type A/D converters which require a plurality of clock cycles to convert, said providing comprising providing different data to different A/D converters at different times, such that output digital values are available at staggered different times.

23. A method as in claim 22, wherein each A/D converter requires N cycles to make a conversion, and wherein there are N of said A/D converters offset in conversion by one clock cycle.

24. An image sensor system, comprising:

a semiconductor substrate;

an array of photoreceptors, arranged on said semiconductor substrate, and arranged to produce analog values indicative of received light energy in a plurality of pixels;

a plurality of successive approximation A/D converters, which require a plurality N of clock cycles to make each conversion, where there are at least N of said successive approximation A/D converters; and

a timing element, providing said analog values to said successive approximation A/D converters in a staggered way, such that at each of a plurality of clock cycles, at least one successive approximation A/D converter produces a digital output.